Docket No.: P2001,0097

CERTIFICATION OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

MAIL STOP: APPEAL BRIEF-PATENTS

By: _____ Date: March 10, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No.	:	10/075,656 Confirmation No.: 9370
Inventor	:	Detlev Richter
Filed	:	February 13, 2002
Title	:	Semiconductor Module with a Configuration for the Self-Test of a Plurality of Interface Circuits and Test Method
TC/A.U.	:	2133
Examiner	:	John J. Tabone, Jr.
Customer No.	:	**24131**

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Sir:

This is an appeal from the final rejection in the Office action dated September 6, 2005, finally rejecting claims 1-13.

Appellants submit this *Brief on Appeal* with payment in the amount of $500.00 to cover the fee for filing the *Brief on Appeal*.

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-13 are rejected and are under appeal.

Status of Amendments:

Appellant's claims 1 - 13 were rejected in a final Office Action mailed September 6, 2005 (the **"final Office Action"**). In response to the **final Office Action**, Appellant filed a Response under 37 C.F.R. § 1.116 on December 6, 2005 (the **"Response"**). No claims were amended after the final Office action

The Primary Examiner stated in an *Advisory Action* dated December 29, 2005 that claims 1-13 had been rejected. The *Advisory Action* further stated, with regard to the

patentability of the claims, that the **Response** did not place the application in condition for allowance because:

> The new arguments presented by the Applicant concerning independent claims 1 and 7 will require further consideration. [emphasis added by Appellant].

A Notice of Appeal was filed on January 10, 2006.

Summary of Claimed Subject Matter:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention relates to a semiconductor module with a plurality of interface circuits and a configuration for the self-test of interface circuits. The application furthermore relates to a method for the self-test of interface circuits of such a semiconductor module.

Appellants explained on page 10 of the specification, line 12, that, referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown a semiconductor module 10 with a logic core 36 and I/O interface circuits 12a, 12b, 14a, 14b, which are assigned terminal pads 22a, 22b, 24a, 24b on the semiconductor module. In this case, in order to make the illustration easier to understand, the schematic illustration of Fig. 1 shows only four I/O interface circuits, whereas in real devices the number of I/O interface devices is generally greater than four, for example 16 or 32.

Appellants stated on page 10 of the specification, line 22, that, the interface circuits 12a - 14b are divided into a first group, containing the interface circuits 12a and 12b, and a second group, containing the interface circuits 14a and 14b. The two groups each have a separate voltage supply. Although all the interface circuits 12a - 14b share the negative supply voltage VSSP (reference symbol 16), the positive supply voltage VDDP1 (reference symbol 18) and VDDP2 (reference symbol 19) is respectively separate for the two groups and embodied via separate terminal pads 28, 29 on the semiconductor chip 10.

Appellants also explained on page 11 of the specification, line 7, that, each group of interface circuits is connected to a linear feedback shift register LFSR (reference symbols 32a, 32b and 34a, 34b, respectively) for generating pseudorandom-distributed test signals. Furthermore, both groups of interface circuits are connected to the common multiple input shift register (MISR) 30. The MISR 30 calculates from received test signals a signature which can be used for checking the correct reception of the test signals.

Appellants also explained on page 12 of the specification, line 4, that, during test operation, first of all the LFSR 34a, 34b generates a series of test signals which are output via the interface circuits 14a, 14b and pass via the connections 52, 54 to the interface circuits 12a, 12b and from there to the MISR 30, which calculates a signature from the test signals. After a specific number of received test signals, the calculated signature is compared with a prescribed signature for fault- free functioning of the interface circuit.

Appellants also explained on page 12 of the specification, line 13, that, afterward, the test direction is rotated, that is to say the LFSR 32a, 32b then generates test signals which are output via the interface circuits 12a, 12b, are received via the connections 52, 54 and the interface circuits 14a, 14b and pass to the MISR 30 for evaluation.

Appellants also stated on page 12 of the specification, line 19, that, in order to achieve high test coverage, the test is multiply iterated and the voltage at the separate power supplies 18, 48 and 19, 49, respectively, for the two interface halves is varied in the process. The separate power supply allows, for example, transmission at high voltage on one half of the interface circuit and reception on the other half of the interface circuit at low voltage.

Appellants further explained on page 13 of the specification, line 18, that, the two interface circuits 112, 114 have a common negative supply voltage VSSP (reference symbol 116) but a separate positive supply voltage VDDP1 (reference symbol 128) and VDDP2 (reference symbol 129), respectively. The LVDS output 114 is connected to an LFSR 132 for generating test signals, and the LVDS input 112 is connected to an MISR 130 for calculating a signature from the received test signals.

Grounds of Rejection to be Reviewed on Appeal

1. Whether or not claims 1 - 5, 7 - 10, 12 and 13 are anticipated by U. S. Patent No. 6,477,674 to Bates et al. ("**BATES**") under 35 U.S.C. §102(e).

2. Whether or not claim 6 is obvious over **BATES** in view of U. S. Patent No. 6,704,897 to Takagi (**"TAKAGI"**) under 35 U.S.C. §103.

3. Whether or not claim 11 is obvious over **BATES** in view of U. S. Patent No. 5,751,151 to Levy et al (**"LEVY"**) under 35 U.S.C. §103.

Argument:

I. Whether or not claims 1 - 5, 7 - 10, 12 and 13 are anticipated by U. S. Patent No. 6,477,674 to Bates et al. ("BATES") under 35 U.S.C. §102(e).

In item 3 of the **final Office Action** mailed September 6, 2005 (the **"final Office Action"**), Appellant's claims 1 - 5, 7 - 10, 12 and 13 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U. S. Patent No. 6,477,674 to Bates et al (**"BATES"**).

Appellant respectfully traverses the above rejections of the claims.

A. Appellant's independent claim 1 is patentable over the BATES reference.

Appellant's claim 1 recites, among other limitations:

> first and second equally sized groups of interface circuits, **wherein each interface circuit of said first group is assigned exactly one interface circuit of said second group**; [emphasis added by Appellant]

As such, Appellant's claim 1 requires, among other things, **a 1:1 correspondence between interface circuits of a first group and interface circuits of a second**

group (i.e., each interface circuit of the first group being assigned to **exactly one** interface circuit of the second group).

Further, Appellant's claim 1 additionally recites, among other limitations:

> **a respective electrical connection of the interface circuits** of said first and second groups **to outside** of the semiconductor module, **for enabling a self-test**; [emphasis added by Appellant]

As such, Appellant's claimed invention requires, among other things, **electrical connections to the first and second interface circuits, for enabling a self-test.**

Appellant believes that the **BATES** reference fails to teach or suggest: 1) Appellant's particularly claimed 1:1 correspondence between the interface circuits of the first and second groups; and 2) the electrical connections from the interface circuits for self-testing.

More particularly, **BATES** discloses a method and apparatus for conducting input/output loopback tests using a local pattern generator and delay elements. **BATES** discloses an integrated circuit including a plurality of I/O buffers, each of which includes an I/O test circuit that generates test pattern signals whenever the integrated circuit is operating in a loopback test mode. See the Abstract of **BATES**. Pages 2 - 3 of the **final Office Action** state, in part:

> The Applicant argues on pages 9 and 10 "However, BATES does not particularly disclose much about these 'other IC 100 devices'. For example, BATES does not particularly disclose whether these 'other IC 100 devices' are arranged in a second group of input/output buffers or if such a 'second group' comprises the same number of input/output

> buffers as the first group . . . .". In response to Applicant's argument the Examiner would like to refer the Applicant back to Figure 5, which is a block diagram of one embodiment of an integrated circuit (IC) 500 that includes input/output (I/O) buffers 100(1)-100(n). I/O buffers 100(1)-100(n) make up a data block of I/O circuitry for transmitting to and receiving data from other IC 100 devices. The "other IC 100 devices" Bates is referring to, **as interpreted by the Examiner**, is a duplication of IC 500 that includes other groups of input/output (I/O) buffers 100(1)-100(n), which qualifies the "other IC 100 devices" as the second group. Bates continues to teach that a data block includes sixteen (16) I/O buffers 100. However, in other embodiments, a data block may include other multiples (e.g., 2, 4, 8, 12, 18, 32, 40, 64, etc.) of I/O buffers 100. (Col. 4, ll.28 - 37). **It stands to reason to one skilled in the art that the I/O buffers 100 (i.e. as well as other IC 100 devices) are groups that are duplicated and therefore, comprises the same number of input/output buffers as the first group.** In light of the arguments presented above, **the Examiner's only conclusion** is that Bates substantially teaches "first and second equally sized groups of interface circuits, wherein each interface circuit of said first group is assigned exactly one interface circuit of said second group;" and "a first circuit connected to said first group and serving to generate test signals to be multiplexed in and output via said interface circuits of said first group; a second circuit connected to said second group for receiving and processing test signals received via said interface circuits of said second group;" [emphasis added by Appellant]

Appellant respectfully traverses the above statement from the **final Office Action**.

BATES does not explicitly state or show that "other IC 100 devices" are I/O devices in equal number to and/or correspond in a 1:1 relationship with the I/O devices 100(1) - 100(n) shown in Fig. 5. This is supported by the above quoted section of the Office Action.

Further, in countering Appellant's arguments to this effect, the Office Action uses such phrases as "**as interpreted by the Examiner**", "**It stands to reason to one skilled in the art that**", and "**the Examiner's only conclusion**", which implies that the standard being used to apply **BATES** to Appellant's claims is one of

obviousness. However, Appellant notes that Appellant's independent claims 1 and 7, including the above limitations, as well as other claims, were rejected under 35 U.S.C. § **102(e)**, which section regards alleged **anticipation** by a reference. As stated in MPEP § 706.02:

> **IV. DISTINCTION BETWEEN 35 U.S.C. 102 AND 103**
>
> The distinction between rejections based on **35 U.S.C. 102** and those based on **35 U.S.C. 103** should be kept in mind. Under the former, the claim is anticipated by the reference. **No question of obviousness is present.** In other words, for anticipation under **35 U.S.C. 102**, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. Whereas, in a rejection based on **35 U.S.C. 103**, the reference teachings must somehow be modified in order to meet the claims. The modification must be one which would have been obvious to one of ordinary skill in the art at the time the invention was made. See **MPEP § 2131 - § 2146** for guidance on patentability determinations under **35 U.S.C. 102** and 103. [emphasis added by Appellant]

As such, it appears that a standard of **obviousness, and not anticipation,** is being applied against Appellant's claims, and it is respectfully requested that the present rejection be reversed.

In response to the above, in the *Advisory Action*, the Examiner stated:

> As for Applicant traversing the Examiner's characterization of certain features in the claims, the Examiner would like to remind the Applicant that the claims are to be given the broadest reasonable interpretation (See MPEP § 2111), which is a requirement of the Examiner for ALL claims and for ALL rejections, 102 or 103. Further, the Examiner never used the phrase "it would be obvious to on [sic] skilled in the art" or any other phrases that would constitute obviousness. As such, the Examiner maintains the rejection as set for [sic] in the Final Office Action of Record dated 08/09/2005 [sic].

Appellant notes that, at least in connection with the 35 U.S.C. § 102(e) rejections of claims 1 and 7, the Examiner did not use the phrase "it would be obvious to one skilled in the art". However, Appellant reiterates that in response to Appellant's previous arguments for the patentability of claims 1 and 7, on pages 2 - 3 of the **final Office Action**, the Examiner stated, among other things that:

> **It stands to reason to one skilled in the art that** the I/O buffers 100 (i.e. as well as other IC 100 devices) are groups that are duplicated and therefore, comprises the same number of input/output buffers as the first group. [emphasis added by Appellant]

(See also the previous discussion, above). As such, although the Examiner did not use the phrase "it would be obvious to one skilled in the art" in connection with claims 1 and 7, the phrase used ("it stands to reason to one skilled in the art that") is a direct synonym, and that the standard being applied to Applicant's claims is one of obviousness, and not anticipation.

However, as stated above, Appellant believes that **BATES** does not teach or suggest that "other IC 100 devices" are I/O devices in equal number to and/or correspond in a 1:1 relationship with the I/O devices 100(1) - 100(n) shown in Fig. 5, if, in fact, a standard of obviousness (i.e., "It stands to reason to one skilled in the art") is being applied to Appellant's claims 1 and 7, Appellant believes that the current rejections be reversed and a new Office Action stating the proper reasons for rejection be issued.

Further, Appellant maintains its belief that the **BATES** reference fails to teach or suggest, among other limitations of Appellant's claim 1, the particularly claimed 1:1

correspondence between the interface circuits of the first and second groups. Page 5 of the **final Office Action** again points to col. 4 of **BATES**, lines 28 - 36, as allegedly disclosing Appellant's particularly claimed first and second equally sized groups of interface circuits. Appellant respectfully disagrees. Col. 4 of **BATES**, lines 28 - 36, states: